Ministry of Higher Education

Al-Zahrawi University

Faculty of Science

Department of Artificial Intelligence Sciences

MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

Module Information معلومات المادة الدراسية					
Module Title	**Logic Design**			**Module Delivery**	
Module Type	**Core**			☒ **Theory** ☐ **Lecture** ☒ **Lab** ☐ **Tutorial** ☐ **Practical** ☐ **Seminar**	
Module Code	ZU-Sc-AI-1A-lo				
ECTS Credits	**5**				
SWL (hr/sem)	**125**				
Module Level		UGI	**Semester of Delivery**		1
Administering Department		Artificial Intelligence	**College**	College of Science	
Module Leader	م.م عادل عبد الباقي		**e-mail**	adil.albari@alzahu.edu.com	
Module Leader's Acad. Title		Assistant teacher	**Module Leader's Qualification**		
Module Tutor			**e-mail**		
Peer Reviewer Name			**e-mail**		
Scientific Committee Approval Date			**Version Number**	1.0	

Relation with other Modules العلاقة مع المواد الدراسية الأخرى			
Prerequisite module	None	**Semester**	
Co-requisites module	None	**Semester**	

Module Aims, Learning Outcomes and Indicative Contents أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية	
Module Objectives أهداف المادة الدراسية	This module aims to: 1. Introduce students to number systems used in digital systems. 2. Develop understanding of Boolean algebra and logic gates. 3. Enable simplification and optimization of logic circuits. 4. Train students to design combinational logic circuits. 5. Introduce sequential logic circuits and memory elements. 6. Strengthen analytical and problem-solving skills in digital logic design.
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	**Upon successful completion of this module, students will be able to:** **LO1:** Explain different number systems and perform conversions between them. **LO2:** Apply arithmetic operations using different number systems. **LO3:** Identify and analyze basic logic gates and Boolean expressions. **LO4:** Simplify Boolean functions using Boolean algebra laws. **LO5:** Minimize logic expressions using Karnaugh Maps with don't-care conditions. **LO6:** Implement Boolean functions using NAND and NOR gates. **LO7:** Design basic combinational logic circuits such as adders and subtractors. **LO8:** Design and analyze decoders, encoders, and multiplexers. **LO9:** Design memory-based combinational circuits such as ROM and PLA. **LO10:** Explain the principles of sequential logic circuits. **LO11:** Analyze and design flip-flops (RS, D, T, JK). **LO12:** Design and analyze registers and basic sequential systems. **LO13:** Apply logic design techniques to solve practical digital circuit problems.
Indicative Contents المحتويات الإرشادية	**Part A – Number Systems and Arithmetic Operations (20 hours)** – Number systems and radix – Decimal, binary, octal, hexadecimal systems – Binary codes (BCD, Gray, Excess-3, ASCII) – Number system conversions – Arithmetic operations – Complements (r, r-1) **Part B – Binary Logic and Boolean Algebra (10 hours)** – Binary logic and logic gates – Truth tables – Boolean algebra laws – Boolean function evaluation – Canonical forms **Part C – Logic Minimization Techniques (14 hours)** – Karnaugh Map structure – K-Maps (2–6 variables)

	– Don’t-care conditions – SOP and POS simplification – NAND and NOR implementations **Part D – Combinational Logic Circuit Design (30 hours)** – Design methodology – Half and full adders – Half and full subtractors – Binary parallel adder – BCD adder – Decoders and encoders – Multiplexers and demultiplexers – ROM and PLA **Part E – Sequential Logic Circuits (15 hours)** – Sequential logic concepts – RS, D, T, JK flip-flops – Registers

Learning and Teaching Strategies استراتيجيات التعلم والتعليم	
Strategies	Teaching strategies include: – Interactive lectures – Hands-on laboratory experiments – Problem-solving exercises – Circuit design demonstrations – Continuous formative feedback These strategies promote analytical thinking and practical circuit design skills.

Student Workload (SWL) الحمل الدراسي للطالب محسوب لـ ١٥ اسبوعا			
Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	79	**Structured SWL (h/w)** الحمل الدراسي المنتظم للطالب أسبوعيا	5.3
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	46	**Unstructured SWL (h/w)** الحمل الدراسي غير المنتظم للطالب أسبوعيا	3.1
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	**125**		

Module Evaluation تقييم المادة الدراسية

		Time/Number	Weight (Marks)	Week Due	Relevant Learning Outcome
Formative assessment	**Quizzes**	2	5% (10)	4 and 10	LO1–LO3, LO7–LO9
	Assignments	2	5% (10)	7 and 12	LO1–LO6, LO7- LO10
	Lab.	5	2% (10)	Continuous	All
	Report	1	10% (10)	14	LO11–LO13
Summative assessment	**Midterm Exam**	2 hrs	10% (10)	8	LO1–LO7
	Final Exam/ Lab	1 hr	10% (10)	16	All
	Final Exam	3 hrs	40% (40)	16	All
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus)

المنهاج الاسبوعي النظري

	Material Covered
Week 1	Introduction to numbering systems: Decimal system, Binary system, Octal system and Hexadecimal system.
Week 2	Introduction to number base conversion: Conversion from decimal system to another system, Conversion from another system to decimal, conversion between all number system.
Week 3	Arithmetic Operations: binary arithmetic operations and arithmetic operation in other systems. The Complement: r and (r-1) complement, Subtraction with (r) and (r-1) complement.
Week 4	Binary codes: BCD, Excess-3, Gray code and other codes. Binary Logic and Logic Gates: Basic gates and Boolean algebra. Boolean Function evaluation and complement Functions.
Week 5	Implement the Boolean Function: Some of Minterms (S.O.M & Product of Maxterms (P.O.M). Minimization of logic circuits using K-Map using 2, 3, 4 and 5 variables in Product of Sum Simplification and Sum of Product Simplifications forms.
Week 6	Don't care conditions: Simplification the Boolean functions in S.O.P and P.O.S forms using don't care conditions. Basic Gates with NAND and NOR gates. Implement Boolean Function using NAND and NOR gates.
Week 7	Mid-term Exam
Week 8	Introduction to combinational logic circuits. Design the basic combinational logic circuits: Adders: design half and full adder, Binary Parallel Adder, BCD adder
Week 9	Combinational logic circuits: design the basic combinational logic circuits: Subtractors: Design half and full subtractor circuits using r and (r-1) complement.
Week 10	Combinational logic circuits: design the basic combinational logic circuits: Decoder and Encoder
Week 11	Combinational logic circuits: design the basic combinational logic circuits: Multiplexer and Demultiplexer.
Week 12	Combinational logic circuits: design different logic combinational circuits: Code converter, Read Only Memory (ROM), and programmable Logic Array (PLA)
Week 13	Sequential Logic Circuits: Flip Flops (RS, D Flip-Flops)
Week 14	Sequential Logic Circuits: Flip Flops (T and JK Flip-Flops).

Week 15	Sequential Logic Circuits: Registers.
Week 16	**Preparatory week before the final Exam**

Delivery Plan (Weekly Lab. Syllabus) المنهاج الاسبوعي للمختبر	
	Material Covered
Week 1	Lab 1: Basic logic Gates (AND, OR, and NOT gates)
Week 2	Lab 2: logic Gates (NAND, NOR)
Week 3	Lab 3: combination gates with examples
Week 4	Lab 4: Digital logic circuits analysis and converting Boolean expressions to digital circuits
Week 5	Lab 5: Boolean algebra and Simplification of Boolean expressions (Part I)
Week 6	Lab 6: Boolean algebra and Simplification of Boolean expressions (Part II)
Week 7	Lab 7: Mid-Term Exam
Week 8	Lab 8: DE Morgan's Theory
Week 9	Lab 9: DE Morgan's Theory and the Universal Gates (part I)
Week 10	Lab 10: DE Morgan's Theory and the Universal Gates (part II)
Week 11	Lab 11: XOR and XNOR gates: Basics and Applications
Week 12	Lab 12: Implementing Half-Adder and Half-Subtractors circuits
Week 13	Lab 13: Implementing Full-Adder and Full-Subtractors circuits
Week 14	Lab 14: Simplification of Boolean expressions – II
Week 15	Lab 15: Review on Logic circuits
Week 16	Course Final Exam

Learning and Teaching Resources مصادر التعلم والتدريس		
	Text	**Available in the Library?**
Required Texts	M Morris R. Mano and Michael D. Ciletti, Digital Design: With an Introduction to the Verilog HDL, VHDL, and SystemVerilog, Pearson, 6th edition, 2018	Yes
Recommended Texts	A.F.Kana, "Digital Logic Design", 2012	Yes
Websites	Online video lectures: https://www.youtube.com/watch?v=N9NNmjpZaGg&list=PLlCTN_xRLDd7k06SMWNpx_FLrqkk1fcVt	

Grading Scheme مخطط الدرجات				
Group	**Grade**	التقدير	**Marks %**	**Definition**
Success Group (50 - 100)	**A -** Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX –** Fail	راسب (قيد المعالجة)	(45-49)	More work required but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required

Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.